AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A semiconductor device for ~~performing an N-bit prefetch operation~~ receiving a plurality of input data to output an N-bit output data at one clock, N being a positive integer, comprising:

a data strobe buffering means for generating N number of align control signals based on a data strobe signal and ~~a~~ an external clock signal;

a receiving block in response to N-1 number of the align control signals for receiving ~~N-bit~~ the plurality of the input data and outputting ~~the~~ intermediate N-bit data in a parallel fashion; and

~~a~~ an outputting block in response to the remaining align control signal for receiving the intermediate N-bit data in the parallel fashion and ~~synchronizing~~ outputting the intermediate N-bit data in synchronization with the remaining align control signal having ~~a~~ an N/2 external clock period to ~~thereby generating~~ generate the synchronized intermediate N-bit data as ~~a prefetched~~ the N-bit output data.

2. (Currently Amended) The semiconductor device as recited in claim 1, wherein the data strobe buffering means generates the N number of align control signals, each having ~~a~~ an N/2 external clock period.

3. (Original) The semiconductor device as recited in claim 2, wherein the receiving block includes N-1 number of latch blocks in response to the N-1 number of the align control signals.

4. (Original) The semiconductor device as recited in claim 3, wherein N is 4.

5. (Currently Amended) The semiconductor device as recited in claim 4, wherein the receiving block includes:

a first latching block for receiving 2-bit data and ~~synchronizing~~ outputting the 2-bit data in synchronization with a first align control signal to ~~thereby generating~~ generate the synchronized 2-bit data as a first synchronized data;

a second latching block for receiving the first synchronized data and ~~synchronizing~~ outputting the first synchronized data in synchronization with a second align control signal to ~~thereby generating~~ generate the synchronized ~~2-bit~~ data as some of the intermediate N-bit data; and

a third latching block for receiving 2-bit data and ~~synchronizing~~ outputting the 2-bit data in synchronization with a third align control signal to ~~thereby generating~~ generate the synchronized 2-bit data as the other of the intermediate N-bit data.

6. (Currently Amended) The semiconductor device as recited in ~~claim~~ [[4]]claim 5, wherein each of the first to third latching blocks includes at least one latch for synchronizing 1-bit data with one of the align control signals.

7. (Currently Amended) The semiconductor device as recited in ~~claim~~ [[4]]claim 3, wherein the data strobe buffering means includes:

an instruction decoder for generating an initialization pulse in response to the data strobe signal; and

a strobe signal divider for receiving the data strobe signal and generating N number of the align control signals based on the strobe signal sequence,

wherein the strobe signal divider is initialized by the initialization pulse.

8. (Original) The semiconductor device as recited in claim 7, wherein the strobe signal divider includes:

first to forth strobe pulse generators, each for receiving the data strobe signal and generating the align control signals based on the strobe signal sequence; and

an initial setting block for initializing the first to forth strobe pulse generators,

wherein the align control signal has the N/2 external clock period.

9. (Original) The semiconductor device as recited in claim 7, wherein the data strobe buffering means includes a latency shifter coupled between the instruction decoder and the strobe signal divider for delaying the initialization pulse for a predetermined time.

10. (Currently Amended) The semiconductor device as recited in claim 7, wherein the data strobe buffering means includes a strobe signal buffer for receiving the data strobe signal and outputting the data strobe signal to the strobe signal divider.

11. (Currently Amended) The semiconductor device as recited in claim 1, wherein the data strobe buffering means generates the N number of align control signals, at least one having ~~a~~ an N/2 external clock period.

12. (Original) The semiconductor device as recited in claim 11, wherein the receiving block includes N-1 number of latch blocks in response to the N-1 number of the align control signals.

13. (Original) The semiconductor device as recited in claim 12, wherein N is 4.

14. (Currently Amended) The semiconductor device as recited in claim 13, wherein the receiving block includes:

a first latching block for receiving 2-bit data and ~~synchronizing~~ outputting the 2-bit data in synchronization with a first align control signal to ~~thereby generating~~ generate the synchronized 2-bit data as a first synchronized data;

a second latching block for receiving the first synchronized data and ~~synchronizing~~ outputting the first synchronized data in synchronization with a second align control signal to ~~thereby generating~~ generate the synchronized ~~2-bit~~ data as some of the intermediate N-bit data; and

a third latching block for receiving the synchronized 2-bit data outputted from the second latching block and ~~synchronizing~~ outputting the 2-bit data in synchronization with a third align control signal to ~~thereby generating~~ generate the synchronized 2-bit data as the other of the intermediate N-bit data.

15. (Original) The semiconductor device as recited in claim 14, wherein each of the first to third latching blocks includes at least one latch for synchronizing 1-bit data with one of the align control signals.

16. (Cancelled)

17. (Currently Amended) The semiconductor device as recited in claim ~~13~~ 12, wherein the data strobe buffering means includes:

an instruction decoder for generating an initialization pulse in response to the data strobe signal; and

a strobe signal divider for receiving the data strobe signal and generating N number of the align control signals based on the strobe signal sequence,

wherein the strobe signal divider is initialized by the initialization pulse.

18. (Original) The semiconductor device as recited in claim 17, wherein the strobe signal divider includes:

first to forth strobe pulse generators, each for receiving the data strobe signal and generating the align control signals based on the strobe signal sequence; and

an initial setting block for initializing the first to forth strobe pulse generators,

wherein the align control signal has the N/2 external clock period.

19. (Original) The semiconductor device as recited in claim 17, wherein the data strobe buffering means includes a latency shifter coupled between the instruction decoder and the strobe signal divider for delaying the initialization pulse for a predetermined time.

20. (Currently Amended) The semiconductor device as recited in claim 17, wherein the data strobe buffering means includes a strobe signal buffer for receiving the data strobe signal and outputting the data strobe signal to the strobe signal divider.

21. (Currently Amended) The semiconductor device as recited in claim 1, wherein the outputting block includes N number of latches, each for synchronizing the intermediate N-bit data with the remaining align control signal having the N/2 external clock period to generate the synchronized intermediate N-bit data as the ~~prefetched~~ N-bit output data.

22. (Currently Amended) The semiconductor device as recited in claim 1, further comprising a global input-output driver for generating the ~~prefetched~~ N-bit output data in response to the strobe enable signal.